ABSTRACT OF THE DISCLOSURE

Disclosed is a vector indexed memory unit and method of operation. In one embodiment a plurality of values are stored in segments of a vector index register. Individual ones of the values are provided to an associated operator (e.g., adder or bit replacement). Individual ones of the operators operates on its associated vector index value and a base value to generate a memory address. These memory addresses are then concurrently accessed in one or more memory units. If the data in the memory units are organized as data tables, the apparatus allows for multiple concurrent table lookups. In an alternate embodiment, in addition to the above described operators generating multiple memory addresses, an adder is provided to add the base value to the value represented by the concatenation of the bits in the vector index register to generate a single memory address. Multiplexers controlled by a programmable mode select signal are used to provide either the multiple memory addresses or the single memory address to the memory units. This alternate embodiment provides an apparatus that can programmably function in either an vector indexed memory mode or a conventional memory addressing mode.